3010a Programmable Frequency Divider

- 5MHz to 2GHz input
- Rugged milled aluminum housing
- RFI shielded construction
- EMI/EMC enhanced circuitry
- ESD protected
- Accepts input signal <-30dBm
- 50Ω RF outputs
- Multiple 3.3V CMOS TTL compatible outputs
- TTL division ratios down to 512 available
- Suitable for frequency synthesis, clock division, clock distribution in electro-optical, molecular spectroscopy, particle physics, and other lab use.

The **Valon 3010a** accepts a wide range of input frequencies and provides three independent, user-selectable, divided outputs. The 3010a is useful for extending the low-frequency range of any signal source down to 5MHz as a 50Ω output or down to 0Hz as a TTL output.

The sixteen available output division ratios are set by the user with hardware jumpers. The division ratios available are: 1,2,3,4,5,6,8,9,10,12,15,16,18,24,30,32. The divide-by-1 setting is useful for buffering and squaring a low-level RF signal. The two 50Ω outputs and the TTL output can be independently programmed to any of the divider ratios.

The two 50Ω ac coupled outputs are equipped with SMA connectors. The third divider output is a 3.3V CMOS TTL dc coupled signal available at the 2mm header. The third divider output also drives a cascade of 4 divide-by-two stages providing an additional divide by 2,4,8,16.

Any divider can be set to divide-by-1 to provide a convenient buffered and squared version of the input. The **Valon 3010a** divider module is designed to be an easily integratable component into any RF or digital system. The only external requirement is a modest 5V~6V dc power source and input signal.

Description

The RF input is signal is applied to a wideband balun to create a balanced ac coupled signal to the input amplifier. This balun is terminated in a dc coupled 50 ohm termination. DC continuity to ground is set at the input SMA connector. The input signal should not have a dc component.

The input amplifier provides gain to the input signal and isolates the input from any noise from the comparator and dividers. The amplifier output drives the comparator which acts as a slicer to convert the input signal to a digital signal. The output of the comparator is applied to the three divider circuits.

All three divider circuits are completely independent and can be programmed separately. Each divider has a 2-bit, base-4 logic input. Unlike a binary bit, the base-4 logic can have one-of-four levels. Therefore, there are 2^4

settings (16). The settings are selected by the supplied 2mm jumpers (sometimes referred to as shunts). The divider ratio selections are shown in the table.

The output signal from all three dividers is a "square waveform" signal and as with all digital signals will have high harmonic content. The output of divider 1 and 2 is an ac coupled RF signal intended to drive 50Ω RF loads. The output from divider 3 is a 3.3V TTL CMOS dc coupled signal suitable for driving any 3.3V TTL digital load. Divider 3 output also drives a synchronous set of additional binary dividers to provide four more divided outputs Jumper headers OUT1, OUT2, and OUT3 are used to set the division ratios for each divider. Each divider ratio is selected by a 2-bit, base 4 code according to the tables shown. For example: to set a division ratio of 10:1, set the jumper labeled "4" to 2 and then set the jumper labeled "1" to 0.

The divider module is capable of dividing a wide range of input signals from below -30dB to over +13dBm in the range of 5MHz to 2GHz. In the divide-by-1 mode, the module acts as low jitter, zero-crossing threshold detector, buffer amplifier.

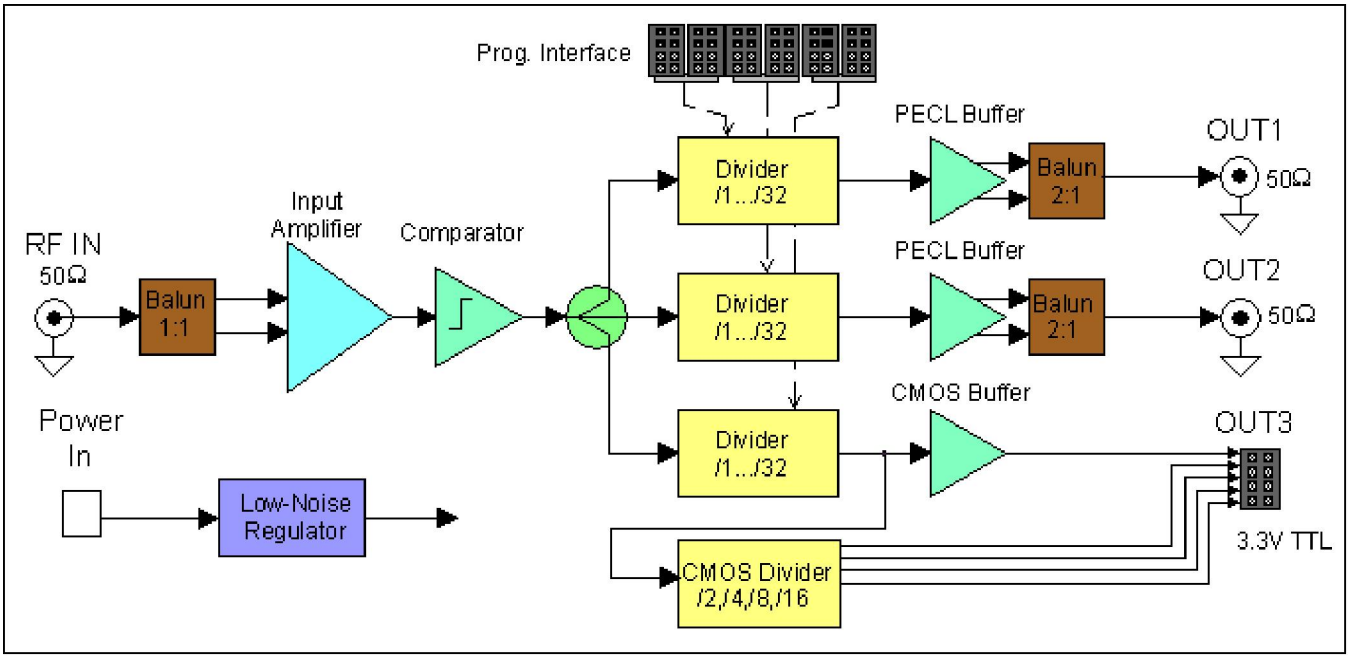

Figure 1 Valon 3010a Functional Block Diagram

Specifications

All specifications are for an operating module case temperature of -25deg.C to +85deg. C.

Power Requirements

Parameter	Min.	Nominal	Max.	Units
Input Voltage	4.0	5-6	9	V
Safe temporary input	-20		+20	V
Input Current	145	150	165	mA

RF Input

Parameter	Min.	typical	Max.	Units	Notes
Input Sensitivity		0		dBm	
100~1000MHz	-20	-35	+13	dBm	
1~2GHz	-10	-20	+13	dBm	
Maximum Input Frequency	1.6	2.0		GHz	0 dBm input
Minimum input Frequency	1.5	3	5	MHz	+10dBm at < 5MHz
Input impedance		50		Ω	
Return Loss	12	15		dB	100MHz to 1GHz
Return Loss	6	10		dB	1GHz ~2GHz
Maximum safe input			20	dBm	

Output Characteristics

Parameter	Min.	typical	Max.	Units	Notes
Frequency Range					
OUT 1 & OUT 2	5	2000	1600	MHz	50Ω Load both ports
	5				
OUT 3-0	0	300	250	MHz	N-0 TTL OUT
OUT 3-1	0	150	125	MHz	N-1 TTL OUT /2
OUT 3-2	0	75	62	MHz	N-2 TTL OUT/4
OUT 3-3	0	37	31	MHz	N-3 TTL OUT/8
OUT 3-4	0	18	16	MHz	N-4 TTL OUT/16
Level					
OUT 1 & OUT 2	3	6		dBm	<500 MHz output
	-3	0		dBm	500~1000MHz output
	-6	-3		dBm	>1000MHz output
Level OUT 3					
TTL Low			0.1	V	3.3kΩ Load
TTL Hi	2.9	3.2		V	3.3kΩ Load

Phase Noise Characteristics

OUT 1 & OUT 2 50Ω Spectral Phase Noise

Parameter	typical	Units	Notes
Divide by 1			
10 Hz Offset	−125		Fin= 622.08 MHz
100 Hz Offset	−132		Fout=622.08 MHz
1 kHz Offset	−140	dBc/Hz	
10 kHz Offset	−148		
100 kHz Offset	−153		
>1 MHz Offset	−154		
Divide by 4			
10 Hz Offset	−128		Fin= 622.08 MHz
100 Hz Offset	−140		Fout=155.52 MHz
1 kHz Offset	−148	dBc/Hz	
10 kHz Offset	−155		
100 kHz Offset	−161		
>1 MHz Offset	−161		
Divide by 8			
10 Hz Offset	−131		Fin= 491.52 MHz
100 Hz Offset	−142		Fout=61.44 MHz
1 kHz Offset	−153	dBc/Hz	
10 kHz Offset	−160		
100 kHz Offset	−165		
>1 MHz Offset	−165		
Divide by 16			
10 Hz Offset	−135		Fin= 622.08 MHz
100 Hz Offset	−145		Fout=38.88 MHz
1 kHz Offset	−158	dBc/Hz	
10 kHz Offset	−165		
100 kHz Offset	−165		
>1 MHz Offset	−166		

OUT 3 TTL Spectral Phase Noise 3.3kΩ load (Output 3-0)

Parameter	typical	Units	Notes
Divide by 1			
10 Hz Offset	−110		Fin= 245.76 MHz
100 Hz Offset	−121		Fout=245.76 MHz
1 kHz Offset	−130	dBc/Hz	
10 kHz Offset	−140		
100 kHz Offset	−145		
1 MHz Offset	−156		
Divide by 4			
10 Hz Offset	−125		Fin= 245.76 MHz
100 Hz Offset	−132		Fout=61.44 MHz
1 kHz Offset	−143	dBc/Hz	
10 kHz Offset	−152		
100 kHz Offset	−158		
1 MHz Offset	−160		

Setting the Division Ratios

The division ratios available are shown in the tables below.

Division Ratio Table for 50Ω Output 1 and Output 2

MSN	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
LSN	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
1&2	1	2	3	4	5	6	8	9	10	12	15	16	18	24	30	32

Division Ratio Table for TTL Output 3

MSN	0	0	0	0	1	1	1	1	2	2	2	2	3	3	3	3
LSN	0	1	2	3	0	1	2	3	0	1	2	3	0	1	2	3
O3-0	1	2	3	4	5	6	8	9	10	12	15	16	18	24	30	32
3-1	2	4	6	8	10	12	16	18	20	24	30	32	36	48	60	64
3-2	4	8	12	16	20	24	32	36	40	48	60	64	72	96	120	128
3-3	8	16	24	32	40	48	64	72	80	96	120	128	144	192	240	256
3-4	16	32	48	64	80	96	128	144	160	192	240	256	288	384	480	512

Any division ratio is user programmable by positioning jumpers on the programming connectors.

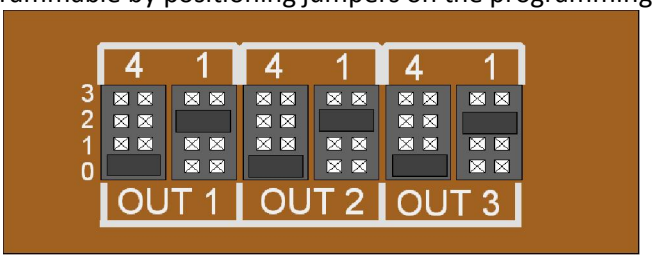

Figure 2 Divider ratio programming by jumper position.

Figure 2 shows the programming selection jumper and header system used to select the desired division ratio. Each divider is programmed according to the tables shown above. By using a base-4 bit system, two jumpers can select one-of-16 values. The headers are 2mm Hirose types and can be used with a cable assembly for remote or embedded programming selection.

Remote control capability is another feature of the Valon 3010a. This can be accomplished in two rather unique ways. One way is to simply replace the jumpers with a contact closure provided by a solid state switch. Another way is provide 2-wire quaternary control for each divider. Figure 3 below shows how to make the connection. Each divider requires two quaternary (four-level) signals reference to ground.

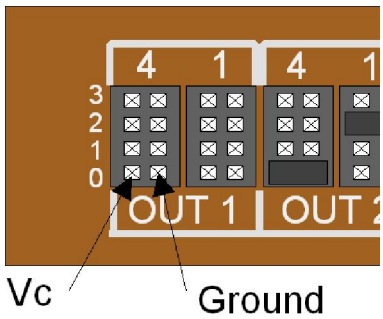

Figure 3 Apply quaternary control for the divider as shown. This is applicable to all dividers.

Quaternary control voltage range

Bit Value	Vc min	Vc max	
0	0.0	0.3	Volts
1	0.7	1.4	
2	1.8	2.6	
3	3.0	3.3	

Note the Vc control voltage can be dc level or a multilevel ac waveform. The waveform can be derived from subsequent dividers or counter to provide duty-cycled control of the division ratios thereby implementing fractional division ratios.

Valon 3010a Programmable frequency dividers can be custom equipped with on-board TCXO so that they can also be used as standalone frequency sources with multiple outputs. For example, several customers use our dividers with a 122.88MHz TCXO installed and set the outputs to provide 122.88 MHz and 61.44MHz. Please contact us to know what your specific requirements are or to place and order.

Interface Connectors

OUT 3 TTL Spectral Phase Noise 3.3kΩ load (Output 3-0)

Function	TYPE	Part No.	Mates with
RF Input, OUT 1, OUT 2	SMA female 50Ω		SMA male 50Ω
DC Power Input	2-position male 2mm pitch	Hirose DF3-2P-2DS	Hirose DF3-2S-2C DigiKey H2023-ND DigiKey pre-crimped wires H2BXT-10112-B4-ND (black) H2BXT-10112-R4-ND (red)
OUT 3	10-position shrouded header 2mm RA	Hirose DF11-10DP-2DS(52)	Hirose DF11-10DS-2C DigiKey H2023-ND DigiKey pre-crimped wires H3BXT-10112-B6-ND (black) H3BXT-10112-R6-ND (red)
Programming Connectors	8-position shrouded header 2mm vert.	DF11-8DP-2DSA(24)	Hirose DF11-8DS-2C DigiKey H2023-ND DigiKey pre-crimped wires H3BXT-10112-B6-ND (black) H3BXT-10112-W6-ND (white)

OUT 3 Connector

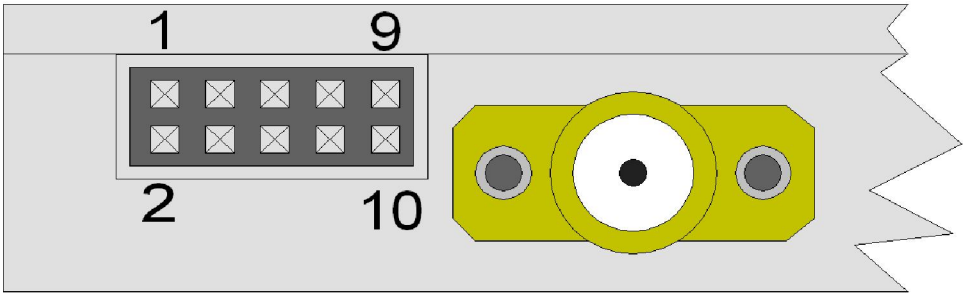

Figure 4 Output 3 Connector Pin Numbering

Pin No.	Description
1	TTL 0UT 3 divided by 16
2	Ground
3	TTL OUT 3 divided by 8
4	Ground
5	TTL OUT 3 divided by 4
6	Ground
7	TTL OUT 3 divided by 2
8	Ground
9	TTL OUT 3
10	Ground

Note: Not all ground wires are necessary. Generally only one or two ground connections are sufficient. The **TTL-1** cable assembly from Valon Technology is available as an optional accessory.

Mechanical Outline Dimensions

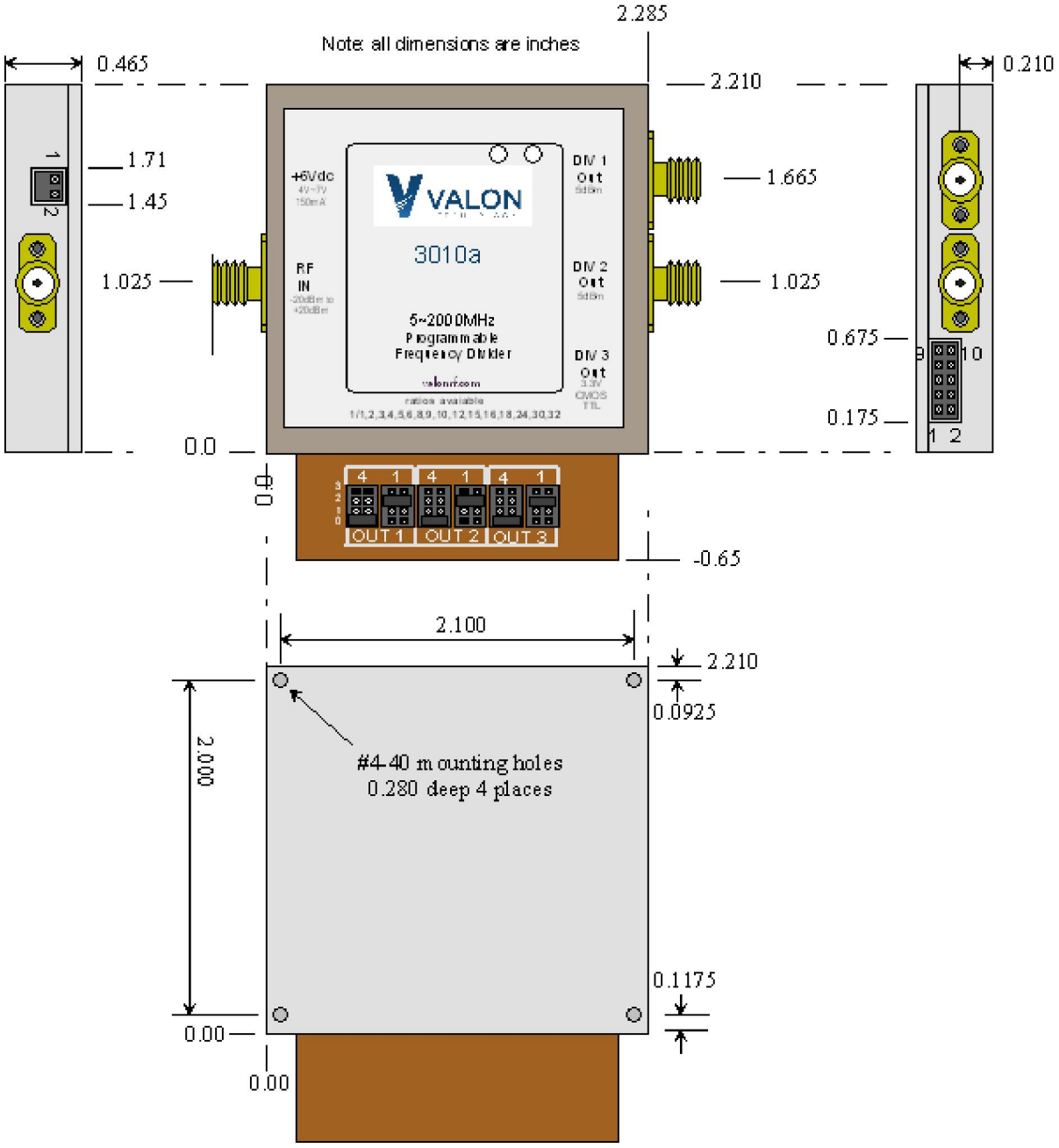

Figure 5 3010a Outline dimensions and mounting hole locations

If you have trouble or need help just contact us.

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